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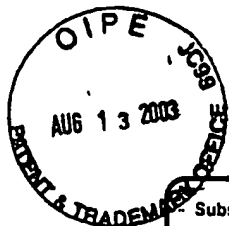
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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	09/954,915
				Filing Date	September 17, 2001
				First Named Inventor	Mark Peting
				Art Unit	2661
				Examiner Name	Unassigned
Sheet	2	of	2	Attorney Docket Number	4259P044

OTHER ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T*
KT		WH YIM and F P COAKLEY, On-Board Processing For KA-Band Applications, University of Surrey, UK, Publication Date, February 11, 1993.	
KT		MARIE-LAURE BOUCHERET, et al., Fast Convolution Filter Banks For Satellite Payloads With On-Board Processing, IEEE Journal on Selected Areas in Communications, Vol. 17, No.2, February 1999.	

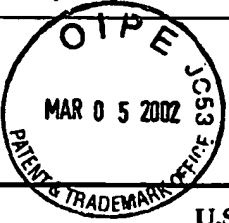
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Based on PTO/SB/08B (05-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 05/02/2003.
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)				Attorney Docket No.: 04259.P044		Application Number: 09/954,915	
				First Named Inventor: Mark Peting		<div style="font-size: 24px; font-weight: bold;">RECEIVED</div> <div style="font-size: 18px; font-weight: bold;">MAR 08 2002</div>	
				Filing Date: September 17, 2001			
U.S. PATENT DOCUMENTS							
Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number	Kind Code ² (If known)				
<div style="font-size: 24px;">↓</div>	KT	6,148,043		Fujimoto	11/14/2000		
		6,141,391		Morelos-Zaragoza, et al.	10/31/2000		
		6,138,265		Morelos-Zaragoza, et al.	10/24/2000		
		6,119,265		Hara	09/12/2000		
		5,974,095		Kitaura, et al.	10/26/1999		
		6,195,642	B1	Izumi, et al.	02/27/2001		
		6,122,325		Mogre, et al.	09/19/2000		
	KT	6,049,573		Song	04/11/2000		
		6,005,640		Strolle, et al.	12/21/1999		

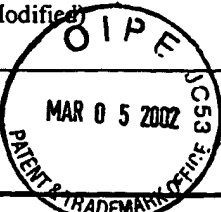
FOREIGN PATENT DOCUMENTS								
Exam. Initial*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD- YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (If known)				

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 04259.P044	Application Number: 09/954,915
		First Named Inventor: Mark Peting	RECEIVED MAR 0 8 2002 Technology Center 2600
		Filing Date: September 17, 2001	
OTHER ART - NO PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
KT ↓ KT		JAMES TSUI, Frequency Channelization, Digital Techniques for Wideband Receivers, Second Edition, Pages 363 - 396, 2001 Artech House, Inc., Norwood, MA	
		ZHENGDAO WANG and GEORGIOS B. GIANNAKIS, Wireless Multicarrier Communications where Fourier Meets Shannon, Department of ECE, University of Minnesota, Minneapolis MN., Pages 1-21	
		E. VERRIEST, ISEN, Implementing an Adaptive Noise Canceling System to Enhance Sonar Receiver Performance Using the TMS320C31 DSP, ESIEE, Paris, September 1996, Texas Instruments, Pages 1-24.	
		G.A. SHAW, R.A. FORD, J.C. ANDERSON, B.W. ZUERDNORFER, A.H. ANDERSON, RASSP Benchmark 2 Technical Description, Massachusetts Institute Of Technology Lincoln Library, 153 pages total.	
		"www.inventra.com/inventra/softcore/workshop/MultiRaFiltDes95/" MENTOR GRAPHICS, Hardware Design of Decimators/Interpolators, Pages 1-38.	
		"www.mentor.com/inventra/softcore/workshop/SDmod95/", MENTOR GRAPHICS, Introduction to AD/DA Converters, Pages 1-27.	
		http://www.mentor.com/inventra/softcore/workshop/SDHWDdes95/ MENTOR GRAPHICS, Design of the Decimation & Interpolation Filters, Pages 1-57.	
		http://www.mentor.com/inventra/softcore/workshop/Applications95/, MENTOR GRAPHICS, Sigma Delta Converter Applications, Pages 1-5.	

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Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	09/954,915
Filing Date	September 17, 2001
First Named Inventor:	Mark Peting
Art Unit	2661
Examiner Name	Not Yet Assigned
Attorney Docket Number	004259.P044

 Sheet 1 of 2
U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
KT		WO	01/59937 A2	8/16/2001	Qualcomm Inc.		

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Substitute for Form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use many sheets as necessary) AUG 1 6 2004 TRADEMARK OFFICE		Application Number	09/954,915
		Filing Date	September 17, 2001
		First Named Inventor:	Mark Peting
		Art Unit	2661
		Examiner Name	Not Yet Assigned
Sheet 2 of 2	Attorney Docket Number	004259.P04 Technology Center 2600	

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
KT		BREE, ET AL., "A Bit-Serial Architecture For A VLSI Viterbi Processor", Communications Systems Research Group, University of Saskatchewan, Saskatoon, IEEE, WESCANEX '88, 1988, pages 72-77.	
		BIVER, ET AL., "Architectural Design and Realization Of A Single-Chip Viterbi Decoder", Elsevier Science Publishers B.V., INTEGRATION, The VLSI Journal 8 (1989), October, No. 1, Amsterdam, NL, Pages 3-16.	
		BREE, ET AL., "A Modular Bit-Serial Architecture For Large Constraint-Length Viterbi Decoding", Communications Systems Research Group, University of Saskatchewan, Saskatoon, Canada, IEEE International Conference on Communications", 1990, pages 1501-1506.	
		CHOI, ET AL., "Viterbi Detector Architecture For High-Speed Optical Storage", 1997, IEEE TENCON - Speech and Image Technologies for Computing and Telecommunications, ASIC Center Corporate Technical Operations SAMSUNG Electronics, Vol. 1, Dec 1997, pages 89-92.	
		W.H. YIM and F.P. COAKLEY, "On-Board Processing For KA-Band Applications", University of Surrey, UK, Publication Date, February 11, 1993., XP 000458011, pp. 225-229.	
KT		HASHIDA MITSUYOSHI, "Hierarchical Network Management System and Control Method for Network Management Information," Patent Abstracts of Japan, Publication No. 07226777	

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